UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,303	12/26/2000	Tsutomu Sasaki	001715	2061

23850 7590 05/01/2006

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
ELLIS, KEVIN L	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,303	SASAKI ET AL.	
	Examiner	Art Unit	
	Kevin L. Ellis	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/7/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-4 are presented for examination. This Office Action is in response to the Amendment filed 4/7/06.

Claim Rejections – 35 USC § 103

2. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Robinson et al., U.S. Patent 5,428,579, in view of Kawasaki et al., U.S. Patent 6,332,196, Jenkin et al., U.S. Patent 5,940,444, and Kawahara, "20-Mb/s Erase/Record Flash Memory by Asymmetrical Operation", 1996.

A) As to claims 1, 2, and 4, Robinson et al. discloses the invention substantially as claimed. There is a data reproduction device (the personal computer 101 shown in figure 1) that comprises a control circuit for reading out data recorded on a memory card (the "memory card" is shown as 110 in figure 1; the "control circuit" would be circuitry in personal computer 101 which would allow communication with the memory card when connected to the computer through connection 112) having a controller mounted thereon (Robinson et al. teaches at Col 5 Lines 10-12 that the memory card includes a controller. This controller can also be considered the "first control means to read out the data from the memory card" which is claimed at line 10), and a data processing circuit for giving

required processing to the read data and outputting the generated data (personal computer 101 contains a microprocessor/CPU that would be the "data processing circuit"). Robinson et al. also teaches that the controller of the memory card can operate the card under two current consumption modes, an active and a standby mode (see Col 2 Lines 6-12 and Line 50 to Col 3 Line 49). The memory card operates in the active mode when it is being read or written to and in the standby mode when no operation is occurring to the memory card. The standby mode operates with a non-zero current consumption for a second current value less than the first current value (see Col 9 Lines 3-54). This results in the same power savings as the present invention. However, Robinson et al. does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode.

Kawasaki et al. teaches a buffer that is utilized similarly to the claimed buffer. The buffer of Kawasaki et al. stores data from a storage device and when the buffer contains sufficient data the storage device is operated in a lower power mode. When the amount of data falls below a threshold the storage device is operated in an active mode and data is read into the buffer (see Abstract and Col 3 Lines 5-45). The buffer of Kawasaki et al. would also inherently include a "control means" to control reading from and writing to the buffer, thus meeting the "second control means to read out the data stored in the buffer" limitation at lines 11-12. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Kawasaki et al. in the system of Robinson et al. and provide a buffer between the

memory card and the requestor of the data. The operation of the memory card would operate in a manner similar to that of the storage device taught by Kawasaki et al. When there is sufficient data in the buffer the memory card can be operated in a reduced power state, when the amount falls below a threshold the memory card would be operated in the powered up state (active mode) and data read into the buffer. This arrangement would provide power savings because the amount of time the memory card operated in a powered on state (active mode) would be decreased.

As for the limitation regarding "read out the data from the memory card at a first bit rate to store the generated data to the buffer ... read out the data stored in the buffer at a second bit rate less than the first bit" (Claim 1 Lines 10-12), these limitations would be inherently met by the teachings of Kawasaki et al. that are combined with the teachings of Robinson et al. There are only three scenarios possible with regard to the data transfer rates of the memory and that of the buffer:

1. memory date transfer rate < buffer data transfer rate
2. memory date transfer rate = buffer date transfer rate
3. memory date transfer rate > buffer date transfer rate

In order for the power savings Kawasaki et al. discloses to happen, the only scenario that can be true is the third one. With the first and second scenario the buffer would never fill up with data because it is being read out of the buffer at a greater or equal to date transfer rate than data is being read from the memory. This would mean that the memory would always be powered on in order to access more data. With the third scenario since the date transfer rate of the memory is greater then the date transfer rate of the buffer, the buffer can be filled with data and then read from the buffer while the

memory is powered down resulting in a power savings. Thus the combination of Robinson et al. and Kawasaki et al. would meet the claimed differences in bit rates of the memory and buffer as the claimed bit rates (buffer bit rate being less than the memory bit rate) is the only scenario possible that would allow for the power savings taught by Kawasaki et al.

Applicant has now amended the claim so that the first bit rate is 8 Mbps and that the second bit rate is 128 Kbps, this being the only modification to the claim language. While the modification to the claim language does narrow the scope of the claim, it merely limits the claim to a subset of what was claimed before. Previously the claim was only limited to a "*first bit rate*" and a "*second bit rate less than the first bit rate*". The previous claim language would cover a wide range of bit rates, the only limitation being that the second bit rate is less than the first. By limiting the claim language so that the first bit rate is 8 Mbps and the second bit rate is 128 Kbps, Applicant has merely claimed a subset of the broad recitation of the second bit rate being less than the first bit rate. Since the Decision on Appeal filed 2/15/06 decided that the combination of Robinson et al. and Kawasaki et al. taught a wide range of bit rates, specifically having the second bit rate less than the first bit rate, the combination would obviously teach a subset of bit rates limited to the first bit rate being 8 Mbps and the second bit rate being 128 Kbps.

Furthermore, the selection of these specific bit rates is not considered novel by the Examiner. If one were to use the combination of Robinson et al. and Kawasaki et al. for reproducing audio date, having the second bit rate be 128 Kbps would have been obvious. Jenkin et al. teaches that a "compressed data rate of 128 kbps would produce essentially

the same audio quality as a music CD." (see Col 1 Lines 64-66) Applicants admitted prior art states that conventionally known digital audio players would record/reproduced audio at a bit rate of 128 Kbps to produce fine quality sound (see P 1 of Specification). Thus it was known at the time of the invention to select a bit rate of 128 Kbps because this would produce audio of essentially the same quality as a music CD.

Applicant's amendment also limits the first bit rate to 8 Mbps. The specification only states that the memory card has a maximum bit rate of 8 Mbps (see Page 6 Line 17 of Specification). The memory card of Robinson et al. utilizes flash memory (see Col 4 Lines 56-63 of Robinson et al.) but is silent as to the data transfer rate of the flash memory. As shown by Kawahara et al., three years before the present invention, flash memory technology had advanced to where it was possible to transfer data at a bit rate of 20 Mb/s (see Abstract). Thus, being able to transfer data to a flash memory at 8 Mbps is not considered novel by the Examiner.

It is noted that Applicant has not set forth any rationale in the specification of why a combination of 128 Kbps and 8 Mbps provides any unknown advantage over other data bit rates.

B) As to claim 3, Robinson et al. teaches setting the memory card in the standby mode when there is no memory access within a predetermined period of time (see Col 16 Lines 16-24).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
April 28, 2006